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Research and Simulation System for Ferroelectric Multibit Memory Cells

David Gal[1,2], Henrietta Bán [1], Vitaly Gerasimov [3], Andriy Haysak [1], Alexander Molnar [1], Taisiya Tretiakova[1]
[1] Uzhhorod National University, Faculty of Physics, Department of the Physics of Semiconductors, Voloshina str. 54, Uzhhorod 88000, Ukraine, alexander.molnar@uzhnu.edu.ua, https://www.uzhnu.edu.ua
[2] WIGNER Research Center for Physics, Po.Box. 49, 1525 Budapest, Hungary, https://wigner.hu
[3] Mukachevo State University, Faculty of Economics, Management and Engineering, Department of Light Industry, Uzhgorodska str, Mukachevo 89600, Ukraine, vitgerv@gmail.com, https://msu.edu.ua

***Abstract* — This paper describes an automated-measurement system of dielectric hysteresis loops, with the ability to measure the parameters of ferroelectric memory cells, both standard properties such as spontaneous polarization, coercive field, bias voltage, as well as such features as switching speed and cell aging. Software control allows not only to automate of the measurement process but also to simulate of the data obtained in order to compensate for conductivity and parasitic capacitance. With its use, the possibility of creating multi-bit ferroelectric memory cells was discovered, which makes it possible to create information storage subsystems of higher density.**

Keywords—ferroelectric; multibit memory cell; measurement system; dielectric hysteresis loop.

I. INTRODUCTION

Recently, Ferroelectric Random Access Memory (FRAM) has been used as a "universal" memory in modern computers and microcontrollers [1]. Memory cells based on ferroelectrics combine the best of Flash and SRAM. It provides non-volatile storage like Flash but offers faster writes, high read-write cycle endurance (>10^{15} cycles), and very low power consumption [2]. Today, they cannot yet replace flash memory and dynamic memory only because of the relatively small capacity of the mass-produced devices [3]. However, due to the simplicity of the manufacturing and the possibility of easy integration with existing CMOS technology, its prospects are very good [4]. One of the ways to overcome the relatively low capacity of existing FRAM microchips is the transition to multi-bit memory cells (as in the case of flash memory), for which there is an ongoing worldwide search for promising ferroelectric materials.

Earlier [5] we proposed the use of ferroelectric $Sn_2P_2S_6$ as a material with the ability to store three bits of information in a single cell. It has also been shown previously that the polarization switching time in these materials can be less than 1 ns [6]. In further studies, it was found that this material makes it possible to create memory cells with the ability to store 4 bits in one cell. To provide these studies, we developed a new fully automated measurement system to investigate dielectric hysteresis loops of ferroelectric memory cells in LabView environment based on Virtual Instrument. The system provides the ability to measure the parameters of ferroelectric memory cells, both standard properties such as spontaneous polarization, coercive field, and bias voltage, as well as such features as switching speed and cell aging. Software control allows modeling of the acquired data to compensate for conductivity and parasitic capacitance.

II. DIELECTRIC HYSTERESIS LOOP MEASUREMENT

Ferroelectricity is the phenomenon of spontaneous polarization in a crystal, even in the absence of an external electric field, at a certain temperature range, which can be reoriented by its application. Crystals with inherent ferroelectricity are called ferroelectrics. Ferroelectrics differ from pyroelectrics in that at a certain temperature (the so-called Curie dielectric point) their crystal modification changes and spontaneous polarization disappears. The crystal modification in which spontaneous polarization is observed is called the polar (ferroelectric) phase, and in which it is not observed - the non-polar (paraelectric) phase.

A. *Dielectric hysteresis loop*

The spontaneous polarization of ferroelectric materials implies a hysteresis effect which can be used as a memory function. A characteristic form (Figure 1) of dependence of the ferroelectric polarization P on the applied electric field strength E is a dielectric hysteresis loop.

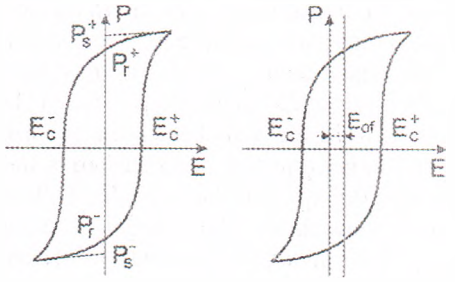

Figure 1. Dielectric hysteresis loops, a) symmetrical, b) asymmetrical.

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The dielectric hysteresis in ferroelectrics is measured using a ferroelectric capacitor (a ferroelectric plate coated with electrodes) and an alternating electric field (varying in a linear or sinusoidal law).

The classical measurement scheme proposed by Sawyer and Tower in 1930 is shown in Fig. 2. [7]

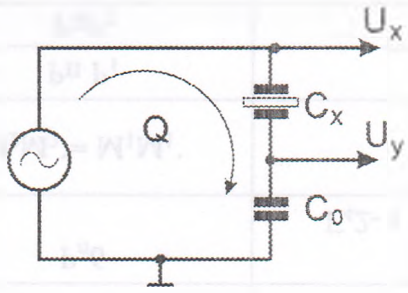

Figure 2. Schematic diagram of dielectric hysteresis loop measurement.

Measurement of the hysteresis loop allows to determine such important integral characteristics of the ferroelectricity as:

1. Spontaneous polarization of P_s
2. Residual polarization P_r
3. Coercive field, E^+_c and E^-_c.

The residual polarization P_r is defined as the polarization value at zero field value. It is less than the maximum measured value P_s by the amount of the dielectric contribution and the part of the total polarization that was switched to the initial state due to spontaneous reverse switching. As can be seen from the figure, the values of the coercive fields are determined at the points of intersection of the hysteresis loop with the $P = 0$ axis. As a rule, the absolute values of the coercive fields for different branches of the hysteresis loop are not equal: $E^+_c \neq E^-_c$, which leads to the appearance of asymmetric hysteresis loops. In this regard, another characteristic is introduced - the bias field, which determines the magnitude of the hysteresis loop shift along the field axis relative to zero. The bias field is an important characteristic because it allows measuring the magnitude of internal electric fields.

B. *Compensation method*

However, when using the classical Sawyer-Tower scheme to study switching loops, the resulting loop often differs significantly from the ideal one. This is due to the fact that in general, the sample under study should be considered as a parallel-connected ferroelectric, dielectric, and conductor. The dielectric component, which includes the parasitic capacitance of the sample and electrodes, increases the polarization (P) and distorts the loop. This component is very large in the case of thin film studies using a tunneling scanning microscope. The component due to conductivity broadens the resulting loop along the P-axis, which manifests itself as the presence of a false polarization even in the paraelectric phase.

One possible method of improving the resulting dielectric hysteresis loops is to connect a variable resistor in parallel with the capacitor on which the charge (or component P) is fixed. By changing its resistance, the best switching loop shape is visually achieved. The advantage of this method is its simplicity, but it also has several very significant disadvantages. The first of them is the ability to compensate only for the conductivity of the sample. The second disadvantage is the impossibility of automating this process due to the lack of a mathematical criterion for the "best" compensation. Therefore, this method was mainly used 10-20 years ago.

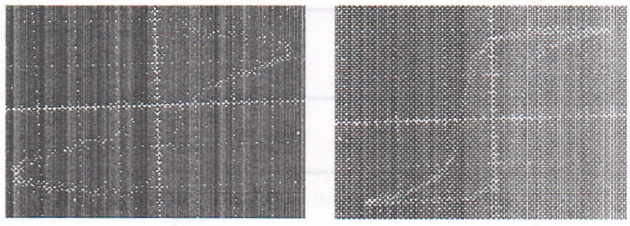

Figure 3. Uncompensated and compensated hysteresis loop in $Sn_2P_2S_6$ at room temperature.

C. *Mathematical compensation of conductivity*

To compensate for the parasitic resistance and parasitic capacitance of the sample, the authors of [8] proposed a software compensation that is much simpler and better than the hardware implementation described in the previous section.

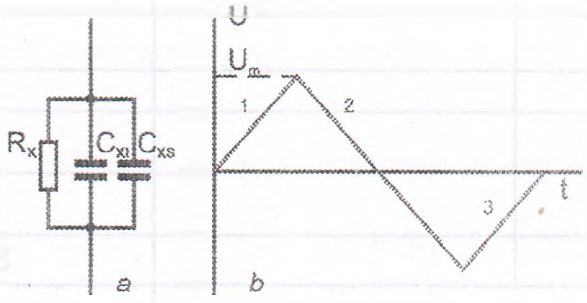

Figure 4. Equivalent circuit of the sample and test wave form [8]

To establish the software compensation criterion, the equivalent circuit of the sample is considered as parallel-connected C_{xi} - parasitic capacitance, C_{xs} - nonlinear capacitance and R_x - equivalent resistance (Fig. 4a). In the case of using a triangular signal, as shown in Fig. 4b, the compensation formula is as follows:

$$E'_1=E_1-C_{xi}U/C_0-U^2/2R_xC_0\beta \quad (1)$$

$$E'_2=E_2-C_{xi}U/C_0+U^2/2R_xC_0\beta-U^2_m/R_xC_0\beta \quad (2)$$

$$E'_3=E_3-C_{xi}U/C_0-U^2/2R_xC_0\beta \quad (3)$$

where E_1, E_2, and E_3 are uncompensated signals, and E'_1, E'_2, and E'_3 are compensated. β is the output voltage ramp rate.

R_x and C_{xi} can be obtained from the saturated branch of the loop, where the domain process does not yet introduce additional polarization. We can set two initial resistances R_1 and R_2 and two initial capacitances C_1 and C_2, so that R_1 and C_1 overcompensate the loop and R_2 and C_2 undercompensate it. By selecting R_1, R_2 and C_1, C_2 by software, we can get the best compensation resistance R_x and capacitance C_{xi}.

The two branches of the compensated loop can be fitted to the modified Weiss equation. According to the Weiss model [9]:

$$P=N\mu\, th\,(\mu(E+bP)/kT) \qquad (4)$$

where μ is the dipole moment, N is the number of dipoles per unit volume, b is a constant, and k is the Boltzmann constant.

Taking into account the nonlinear relationship between polarization and electric field, the repolarization of domains will be described by the modified Weiss formula:

$$P = th\,(a_0+a_1E+a_2E^2+a_3E^3+b_1P+b_2P^2) \qquad (5)$$

a_0, a_1, a_2, a_3 and b_1, b_2 are coefficients, P and E are normalized values of polarization and electric field, P' and E' are their measured values.

$$P=P'/P'_m \text{ та } E=(E'-E'_c)/E'_m \qquad (6)$$

where P'_m is the spontaneous polarization, E'_c is the coercive field, and E'_m is the maximum value of the electric field.

Using these formulas, it is possible to approximate any experimental repolarization loops.

D. Method of excitation signal modification

A more modern method is to modify the excitation signal applied to the test sample (practically the same classical Sawyer-Tower scheme is used).

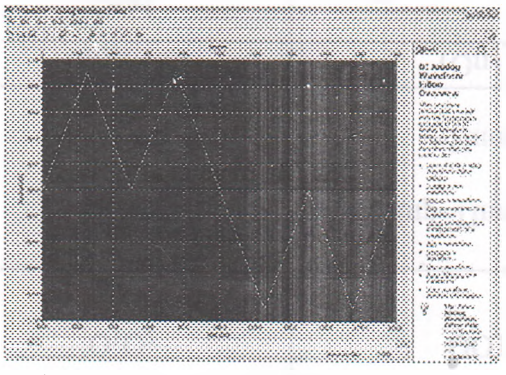

Figure 5. Double triangle excitation waveform

In this case, instead of a sinusoidal signal, a triangular, double triangular, or a set of rectangular signals are used, the amplitude and width of which vary according to a sinusoidal law. The most sophisticated of these excitation signals is the double triangular signal [10].

The method of double triangular excitation signal (Fig. 5), by applying a unipolar triangular signal twice to the sample instead of a sinusoidal signal used in the classical Sawyer-Tower scheme (Fig. 2), allows us to obtain a second switching loop due to the second half-wave of excitation, in which all the parasitic components of the sample under study are concentrated (as shown in Fig. 6*a*). By mathematically subtracting these loops from each other (Fig. 6*b*), we obtain an ideal switching loop that does not contain components caused by the sample conductivity and its parasitic capacitance. No manual compensation is used, and the whole process is very well and easily automated.

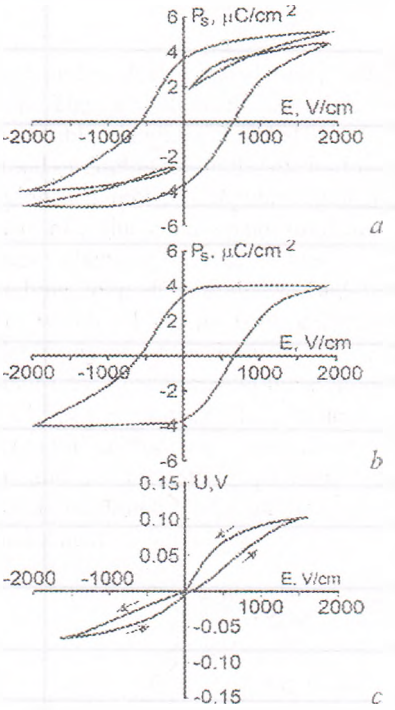

Figure 6. Measured (*a*) and reconstructed (*b*) dielectric hysteresis loop of $Sn_2P_2S_6$ crystal at room temperature and 10 Hz switching field frequency. (c) Voltage dependence on the reference capacitor Co (2.2 μF). Arrows show the course of the applied voltage change..

To evaluate the performance of the method, a single crystal of $Sn_2P_2S_6$ of polar cut with a thickness of d = 0.06 cm and an electrode area (In-Ga eutectic) of S = 0.28 cm^2 was used. The resulting loops before and after treatment are shown in Fig. 6.

Using the data on the parameters of the measured circuit and the sample, it is possible to calculate the value of the reversal part of the spontaneous polarization and the effective conductivity of the sample.

Considering that the capacitance of the reference capacitor C_0 = 2.2 μF, the value of spontaneous polarization can be calculated by the formula

$$P=\frac{CU}{S} \quad (7)$$

The spontaneous polarization of $P_s \sim 5$ μC/cm² was somewhat lower than the previously published values (14 μC/cm²) [11]. This may be due to the following reasons. First, there may be areas in the sample where the domains are anchored to defects, and the measured value is only the reverse part of Ps. This is evidenced, in particular, by the asymmetry of the measured loops in the absence of switching, which may be due to the partial unipolarity of the sample. Secondly, the small thickness of the sample (0.6 mm) may be the reason that a significant part of the volume is in the shielded state (large volume at the electrode layer) and also does not participate in the switching processes. Finally, the deviation may be caused by an inaccurate orientation of the sample, i.e., the deviation of the normal to the surface of the crystal plate from the polar direction. The value of the coercive field (about 600 V/cm) correlates well with the literature data [12].

The effective electrical conductivity of the sample can be estimated from the data shown in Fig. 6*c*. Indeed, in the absence of switching processes, the voltage increases on the reference capacitor C_0 (in the case when the voltage change occurs much faster than the discharge of the capacitor) can be estimated from the ratio $J=(C/S)\cdot(\Delta U/\Delta t)$, i.e., by the slope of the straight-line section of the curve in Fig. 6*c*. With the reverse course of the applied voltage, this dependence is significantly nonlinear, which is caused by the relatively large value of the discharge time *C*. With a reference capacitor of 2.2 μF and an input impedance of 1 GΩ, the time constant of the input circuits is $2\cdot10^3$ seconds. Using the data of Fig. 6*c*. in the positive ($E > 0$) part of the $U(E)$ dependence. we obtain the value of the effective electrical conductivity $\sigma = J/E = 0.5\cdot10^{-7}$ (Ohm·cm)$^{-1}$, which is in general in good agreement with the values known in the literature for "low-impedance" $Sn_2P_2S_6$ samples [11].

III. Experimental Setup

To study the polarization switching processes, we developed an automated measuring system using the USB 6211 I/O module from National Instruments and created a program to control the process of data acquisition and processing in the LabVIEW graphical environment (Fig. 7).

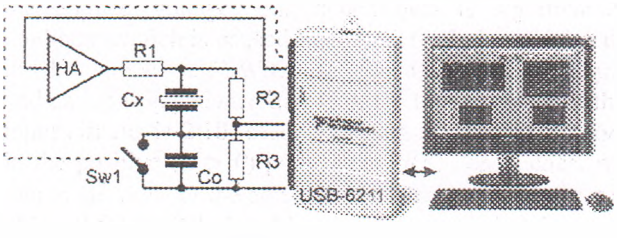

Figure 7. Block diagram of the measuring system for the study of dielectric hysteresis loops.

The software-generated measured signal of arbitrary shape (sinusoidal, triangular, double-triangular, etc.) from the output of the USB 6211 module's digital-to-analog converter is fed to a high-voltage amplifier, from which it is supplied to the classical Sawyer-Tower circuit, which consists of the investigated ferroelectric capacitor C_x and a conventional high-voltage reference capacitor C_0 with low losses and a capacity of 2.2 μF.

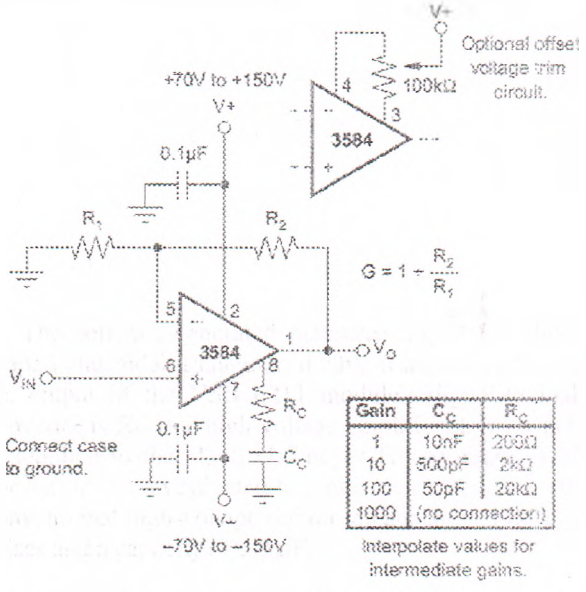

Figure 8. Schematic diagram of a high-voltage amplifier [13].

The resistor R1 serves as a current limiter in the circuit. The measured voltage (scaled by the voltage divider R2 and R3) and the signal from the capacitor C_0 are sent to the two inputs of the USB 6211 module, where, after amplification, they are converted into a digital code using the built-in analog-to-digital converter (ADC) and transmitted to the control computer via the USB interface. This scheme provides for a programmable "zeroing" using an electromagnetic relay connected in parallel to the capacitor C. This allows you to start measurements from the zero value of the charge on the capacitor, and the zero of the generated triangular signal. The high voltage amplifier (HA, Fig. 8.) is based on the Burr-Brown (now Texas Instruments) 3584 high voltage [13] operational amplifier (op amp). This op amp is specially designed for use in systems with capacitive load. It is the only integrated operational amplifier to date that has a maximum output voltage of ±150 volts and an operating frequency range of 60 MHz. The output voltage rise rate of 160 V/μs allows measurements up to 1 MHz with a maximum output voltage swing. In addition, this chip has short-circuit protection on the output, power failure protection, and built-in overheating protection. Thanks to the use of field-effect transistors in the input circuits of this circuit, its input current is very low (20nA), which allows not to load the output of the preliminary stages (in our case, the DAC).

The process of synthesizing the measured signal, collecting and processing the obtained experimental data is controlled by a program created in the LabVIEW graphical environment (Fig. 9).

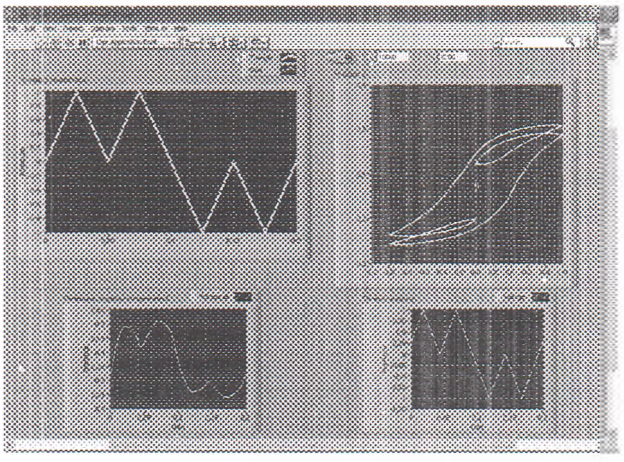

Figure 9. Front panel of the LabVIEW control program of the measuring system for polarization switching study

The main advantage of our system is the digital processing of both the excitation and the detected signal. This makes it possible to use both the method from section II*a* and II*b* to compensate for parasitic capacitance and conductivity in the study of switching processes in ferroelectrics. In addition, using the temperature control subsystem, it is possible to measure the temperature dependence of sample parameters in the range of 80-400K. By replacing the reference capacitor with a reference resistor and the excitation signal with rectangular pulses, we can use the Mertz technique to analyze sample switching current. And long-term measurements make it possible to study the aging processes of a ferroelectric capacitor.

IV. Multibit Memory Cells

Most modern semiconductor memory is of one of two types - dynamic or flash memory. DRAM has a relatively high access speed (worse than static), but requires constant regeneration and the presence of a supply voltage to maintain cell content. Flash memory, has a much higher capacity, is non-volatile, but is much slower and can withstand a limited number of write cycles. Therefore, the *Holy Grail* of modern "universal" memory is a type of memory cells, which should combine all the advantages of modern devices without their disadvantages, namely: high speed (units or fractions of nanoseconds), large or unlimited number of write cycles, be non-volatile, have a very large volume (gigabytes or even better terabytes), have low power consumption. Ferroelectric memory is a contender for this role [2]. Today mass-produced ferroelectric memory has a comparatively small volume, tens of megabytes, although all other parameters make it meet the requirements for "universal" memory.

One method of solving this limitation is the transition to multibit memory cells, as once happened with flash cells. A promising candidate material for ferroelectric memory capacitors is $Sn_2P_2S_6$, whose polarization switching rate can be at the level of picoseconds [6], and three-bit recording technology has been implemented in them [5]. Studies of $Sn_2P_2S_6$ samples revealed polarization switching in the form of double hysteresis loops. This peculiarity is connected with the three-well form of the local potential for spontaneous polarization fluctuations, which determines the possibility of existence of metastable non-polarized regions below the second order phase transition temperature at $T_0 \approx 338$ K. The origin of spontaneous polarization is determined by changes in chemical bonding, which can be represented as a second-order Jan-Teller effect based on stereoactivity of single electron pairs of Sn^{2+} cations and valence vibrations of $P^{4+} + P^{4+} \longleftrightarrow P^{3+} + P^{5+}$ phosphorus cations. This model can explain the coexistence of ferroelectric and antiferroelectric hysteresis loops in $Sn_2P_2S_6$ crystals [5].

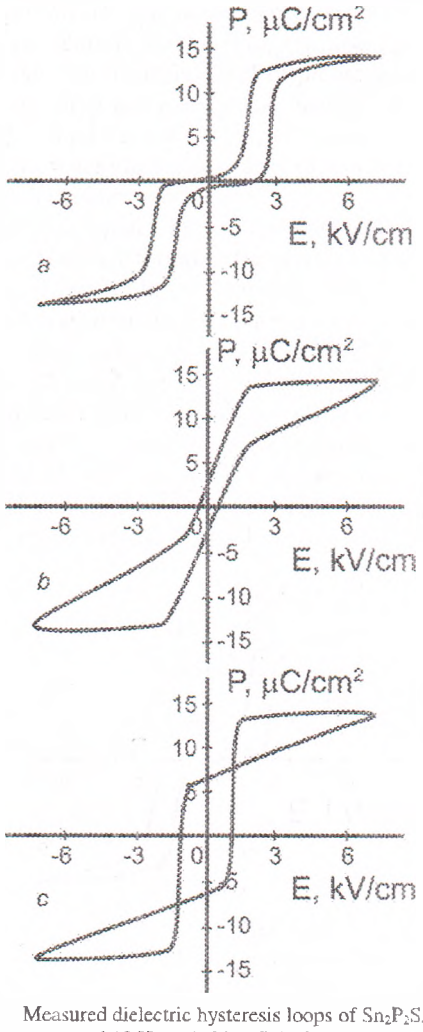

Figure 10. Measured dielectric hysteresis loops of $Sn_2P_2S_6$ crystal at room temperature and 10 Hz switching field frequency and different ratios of ferroelectric and antiferroelectric regions in the crystal volume..

During a study of a $Sn_2P_2S_6$-based ferroelectric capacitor it was found that depending on the ratio of the concentration of ferroelectric and antiferroelectric regions in the crystal, which in turn is determined by the degree of system non-equilibrium (cooling rate and relaxation time), double hysteresis loops characteristic of antiferroelectric (Fig. 10*a,b*) as well as triple hysteresis loops of spontaneous polarization switching (Fig. 10*c*) can be observed. The latter can be used to create memory cells with four stable states, and store 4 bits in one memory cell.

V. Conclusions

Digital control and signal processing in the study of switching processes in ferroelectrics make it possible to compensate for the parasitic capacitance and conductivity of samples, improving the quality of the data that is obtained. Using an automated measuring system, it is possible to study the temperature and time dependencies of the parameters of a ferroelectric capacitor or memory cell, concluding the aging processes and the possibility of using the cell in a wide range of operating temperatures.

The data we obtained on the switching processes of an $Sn_2P_2S_6$-based ferroelectric capacitor showed that, under certain conditions, double and triple dielectric hysteresis loops can be observed in them, indicating that multibit memory cells capable of storing 3 or 4 bits can be created based on these materials.

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89600, м. Мукачево, вул. Ужгородська, 26
тел./факс +380-3131-21109
Веб-сайт університету: www.msu.edu.ua
E-mail: info@msu.edu.ua, pr@mail.msu.edu.ua
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